REMARKS/ARGUMENTS

Claims 1-4 remain pending in the application.

Claims 1-4 are rejected under 35 U.S.C. §103 as being unpatentable over the combination of *Hwang et al.* (EU-0614226 hereinafter, "*Hwang*"), *Aitken et al.* (US 5,268,324 hereinafter, "*Aitken*") and further in view of *Song* (US 6,451,681).

Applicant has carefully reviewed the cited references and respectfully reiterates his traversal of the Examiner's rejections and asks for favorable reconsideration. Applicant submits that the pending claims are patentable over the cited references.

The Cited References

Hwang provides proper and symmetric threshold voltages suitable for CMOS logic applications, for n-channel and p-channel MOSFETs through the use of a gate electrode structure in which a thin TiN layer is sandwiched in between the gate oxide of the MOSFET and the polysilicon gate portion of the MOSFET. Furthermore, as the Office Action concedes, *Hwang* does not disclose an amorphous silicon formed between the gate oxide layer and the layer of polycrystalline silicon. Also Hwang is characterized in that the gate electrodes of the NMOS transistors are formed in a layer of n-type doped polycrystalline silicon **without** [emphasis added] germanium.

Aitken generally relates to silicon (Si) CMOS transistor technology, and , more particulary to silicon-germanium-based techniques for modifying the Si technology to enhance the performance of the CMOS transistors, particularly the p-channel transistors. *Aitken* also recites a PMOS gate electrode (10) with SiGe and an NMOS gate electrode without SiGe. Both electrodes are stacked directly on top of the silicon substrate (coupled electrically to the silicon substrate via the N-well (7) and P-well (8)). Refer to Fig. 1D.

Song relates to a thin film transistor (TFT) having an improved contact layer and a method for manufacturing the same, and more particulary to a TFT

having a Si-Ge contact layer and a method for manufacturing the same. In FIGS. 3A – 3E, *Song* recites a gate electrode 21 formed on silicon substrate 11.

Applicant's Invention

In contrast with the cited references, Applicant's invention is directed to a "a semiconductor device with an integrated CMOS circuit with NMOS and PMOS transistors having semiconductor zones which are formed in a silicon substrate and which adjoin a surface thereof, which surface is provided with a layer of gate oxide on which gate electrodes are formed at those transistors, such that the gate electrodes of the PMOS transistors are formed in a layer of p-type doped polycrystalline silicon and a layer of p-type doped polycrystalline silicon-germanium (Si$_{1-x}$Ge$_x$; $0<x<1$) situated between said polycrystalline silicon layer and the gate oxide, along with an amorphous silicon layer which is formed, characterized in that the gate electrodes of the NMOS transistors are formed in a layer of n-type doped polycrystalline silicon without germanium."

The §103 Rejections

Claims 1-4

With respect to claims 1-4, Applicant respectfully asserts that the Office Action has not made the case for a §103 rejection. As discussed in the references earlier, *Hwang* failes to teach or suggest the claimed features of Applicant's invention. Hwang requirers that both PMOS and NMOS gate electrodes be stacked on a lyear of TiN. Furthermore, as stated earlier *Aitken* also recites a PMOS gate electrode (10) with SiGe and an NMOS gate electrode without SiGe. Both electrodes are stacked directly on top of the silicon substrate. *Song* recites a gate electrode 21 formed on silicon substrate 11.

Applicant respectfully reiterate that the present rejection is one of classic hindsight reconstruction. It is for this reason that the Court of Appeals has

repeatedly indicated that there must be adequate evidence to corroborate the alleged motivation to modify the teachings of the prior art. Without such evidence, for almost every patent application based on previously known matter, the prior art could be used to reconstruct the invention claimed. The law, however, has safeguards against such Patent Office practice.

First, there must be evidence **in the cited prior art** to corroborate the alleged motivation to modify the teachings of the prior art. *See, e.g., In re Dembiczak*, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999), *Ruiz v. A.B. Chance Co.*, (Fed. Cir., December 6, 2000), that the alleged motivation for combining the references is to be suggested by the ***references*** ("Our court has provided [that the] motivation to combine may be found explicitly or implicitly: 1) in the ***prior art references*** themselves; 2) in the knowledge of those of ordinary skill in the art that certain ***references***, or disclosures in those references, are of special interest or importance in the field; or 3) from the nature of the problem to be solved, 'leading inventors to look to ***references*** relating to possible solutions to that problem.'").

Second, the law indicates that identification of the problem being addressed is an important part of the statutory requirement that the invention be considered "as a whole" when evaluating whether or not §103(a) applies. *See, e.g.,* §103(a), *Graham v. John Deere Co.*, 383 U.S. 1 (1966).

Additional case law in this regard is provided in the MPEP. For example, MPEP § 2112.02 clearly states that, "The discovery of a new use for an old structure based on unknown properties of the structure might be patentable to the discoverer as a process of using." It further provides that "[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. §103." MPEP § 2141.02. In this instance, Applicants have provided a clear assertion of this discovery in the specification:

Applicant's invention address a long felt need to "provide a solution for enabling the formation of a CMOS structure with increasing the speed of PMOS transistors toward the level of that of NMOS by increasing the hole mobility of the PMOS through the inctorudction of of silicon-germanium gate electrodes. Furthermore, this PMOS performance enhancement is accomplished without having the silicon-germanium used in the PMOS affect the NMOS transistor.

The Office Action's assertion that combining the references of *Hwang* and *Aitken* because that *Hwang* "discloses that TiN has the same work function as instrinsic polysilicon"(Office Action, page 4, paragraph 2) would necessarily be equivalent and could be substituted into one wafer fabrication process into another is **not** sufficient motivation to combine the references.

A given wafer fabrication process is a result of experimentation and the combination of many materials and recipes to produce working devices in silicon. Based on these significantly different properties, one of ordinary skill in the art would expect different process to behave quite differently to different materials introduced. Experience has in fact proven this to be the case. One parameter, the work function would not make the case to a process engineer reasonably skilled in the art to subsitute one material for another.

Consequently, the modification of *Hwang*, *Aitken*, and *Song* would destroy the their intended functions and therefore are not proberly combinable. If a prior art reference is cited that requires some modification in order to meet the claimed invention or requires some modification in order to be properly combined with another reference, and such modification destroys the purpose or function of the invention disclosed in the references, one of ordinary skill in the art would not have found a reason to make the claimed modification. See *In re Gordon, 733 F. 2d 900, 221 USPQ 1125 (Fed. Cir. 1984)*. Additionally,MPEP §2143.01 provides:

> **The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior are also suggests the desirability of the combination.** *In re Mills, 916 F.2d 680, 16USPQ2d 1430 (Fed. Cir 1990)*

Applicant requests that the §103 rejections be withdrawn.

Conclusion

In light of the amendments and arguments presented, Applicant believes he has addressed the Examiner's concerns. Therefore, the claims are allowable. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Please charge any fees other than the issue fee and credit any overpayments to Deposit Account 14-1270.

Respectfully submitted,

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